Amendments to the Specification

Please replace the paragraph beginning on page 5, line 9, with the following amended paragraph:

Embodiments of the present invention are directed to a device that improves upon the conventional device, where size (and therefore cost), is important and where the ability to interface with multiple clock domains and perform random accesses and bi-directional accesses is important. In one embodiment, memory device comprises two or more port synchronization logic devices, a port multiplexing logic, and a single-ported memory core. The port synchronization logic devices synchronize information communicated between ports associated with the port synchronization logic devices and the single-ported memory core by synchronizing the information between port clocks and a core clock. The two ports and the core clock can operate at different frequencies. Typically, the core frequency is twice that of the fastest port frequency. In one embodiment, the core frequency is at least twice that of the fastest port frequency.

Please replace the paragraph beginning on page 9, line 5, with the following amended paragraph:

According to another embodiment, device 300 has a port multiplexing logic 370 so that device 300 can operate with multiple ports (~~330, 340~~ 310, 320). According to one embodiment, port multiplexing logic 370 acts as a time division multiplexer (TDM) for data and addresses communicated between the port synchronization logic devices (330, 340) and the single-ported memory core 380. In one embodiment, the core frequency is twice that of the fastest port (310, 320) frequency. In this case, the multiplexing logic 370 may be enabled to "ping-pong" between serving the two ports (310, 320). Of course, other well known time multiplexing techniques could be employed for the other port frequencies.

Please replace the paragraph beginning on page 11, line 4, with the following amended paragraph:

FIG. 4 depicts a port synchronization logic device, e.g., device 330, according to one embodiment of the present invention. According to one embodiment, a port synchronization logic device may use FIFOs to synchronize information that is received and outputted. For example, the port synchronization logic device 440 includes a read data and control FIFO 442 for synchronizing data that is outputted, a write data and control ~~FIFO 444~~ FIFO 446 for synchronizing information that is received, and an address ~~FIFO 446~~ FIFO 448 for synchronizing addresses that are received. Typically, data and addresses are received and supplied at the port side according to the port clock rate, however, data and addresses on bus 454 and 456, as well as, data on bus 452 are at the core frequency.

Please replace the paragraph beginning on page 12, line 10, with the following amended paragraph:

In yet another embodiment, the ~~FIFO's~~ FIFOs (442, ~~444, 446~~ 446, 448) are implemented with memory and/or synchronization registers. According to one embodiment, the read data and control FIFO 442 is only for receiving data from the data read bus 452. Similarly, according to one embodiment, the write data and control ~~FIFO 444~~ FIFO 446 is only for writing data to the data write bus 454.

Please replace the paragraph beginning on page 12, line 16, and ending on page 13, line 3, with the following amended paragraph:

Just as port clocks may be associated with ports 310, 320 in FIG. 3, a port clock may be associated with port 410 depicted in FIG. 4, according to one embodiment. According to another embodiment, the ~~FIFO's~~ FIFOs (442, ~~444, 446~~ 446, 448) are used for synchronizing signals that cross the clock boundary between port 410 and a single-ported memory core. For example, when the port synchronization logic device 440 receives data from port 410 which it ultimately communicates to a single-ported memory core, write data and control FIFO 446 may synchronize the data from port 410's clock to the single-ported memory core's clock (referred to hereinafter as a "core clock"). The data may then be processed with respect to the core clock. Similarly, when the port synchronization logic device 440 receives addresses from port address bus

414, the address FIFO 446 may synchronize the addresses from port 410's clock to the core clock. Further, when the port synchronization logic device 440 receives data from a single-ported memory core which it communicates to port 410, the read data and control FIFO 442 may synchronize the data from the core's clock to port 410's clock.

Please replace the paragraph beginning on page 13, line 5, with the following amended paragraph:

FIG. 5 depicts a port synchronization logic device according to one embodiment of the present invention. The port synchronization logic device 540, as depicted in FIG. 5, is similar to port synchronization logic device 440, depicted in FIG. 4, except that device 540 optimizes for the situation where port 410's clock is half as fast as the core clock by using multiplexers (542, 544, 546) to bypass the ~~FIFO's~~ FIFOs (442, 446, 448). This embodiment may be used when the port clocks and the core clock are generated from the same clock circuit. For example, if port 410's clock is from the same source as the core clock, then data from the buses (452, 412, 414) would flow to the respective multiplexers (542, 544, 546). However, if port 410's clock is not from the same source as the core clock, then data from the control lines (452, 412, 414) would flow to the FIFOs (442, ~~440, 446~~ 446, 448). According to one embodiment, signal control lines (not shown) for each multiplexer (542, 544, 546) select whether or not to bypass the FIFOs (442, 446, 448). These lines may be enabled via configuration states.